

## **DDR3 2G 1600 1.5V SO-DIMM**

2GB 1Rx16 256M x 64-Bit PC3-12800 CL11 204-Pin SODIMM

### **SPECIFICATIONS**

CL(IDD)	11 cycles
Row Cycle Time (tRCmin)	48.125ns (min.)
Refresh to Active/Refresh Command Time (tRFCmin)	260ns (min.)
Row Active Time (tRASmin)	35ns (min.)
Maximum Operating Power	1.170 W*
UL Rating	94 V - 0
Operating Temperature	0₀ C to 85₀ C
Storage Temperature Main Chips	-55₀ C to +100₀ C Samsung.Hvnix.Micron
Main Chips	Samsung,Hynix,Micron

<sup>\*</sup>Power will vary depending on the SDRAM used.

#### **DESCRIPTION**

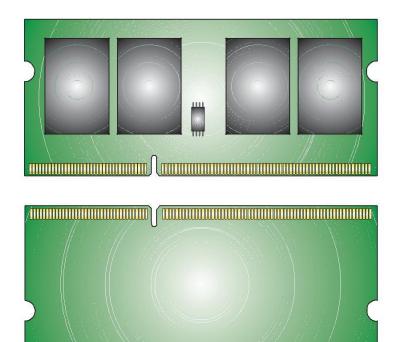
This document describes ValueRAM's 256M x 64-bit (2GB) DDR3-1600 CL11 SDRAM (Synchronous DRAM) 1Rx16, memory module, based on four 256M x 16-bit FBGA components. The SPD is programmed to JEDEC standard latency DDR3-1600 timing of 11-11-11 at 1.5V. This 204-pin SODIMM uses gold contact fingers. The electrical and mechanical specifications are as follows:

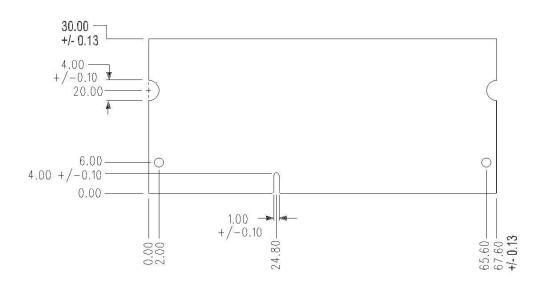
#### **FEATURES**

- JEDEC standard 1.5V (1.425V ~1.575V) Power Supply
- VDDQ = 1.5V (1.425V ~ 1.575V)
- 800MHz fCK for 1600Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 11, 10, 9, 8, 7, 6, 5
- Programmable Additive Latency: 0, CL 2, or CL 1 clock
- · 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE ≤ 95°C</li>
- Asynchronous Reset
- PCB: Height 1.180" (30.00mm), single sided component



# **MODULE DIMENSIONS:**





(units = millimeters)